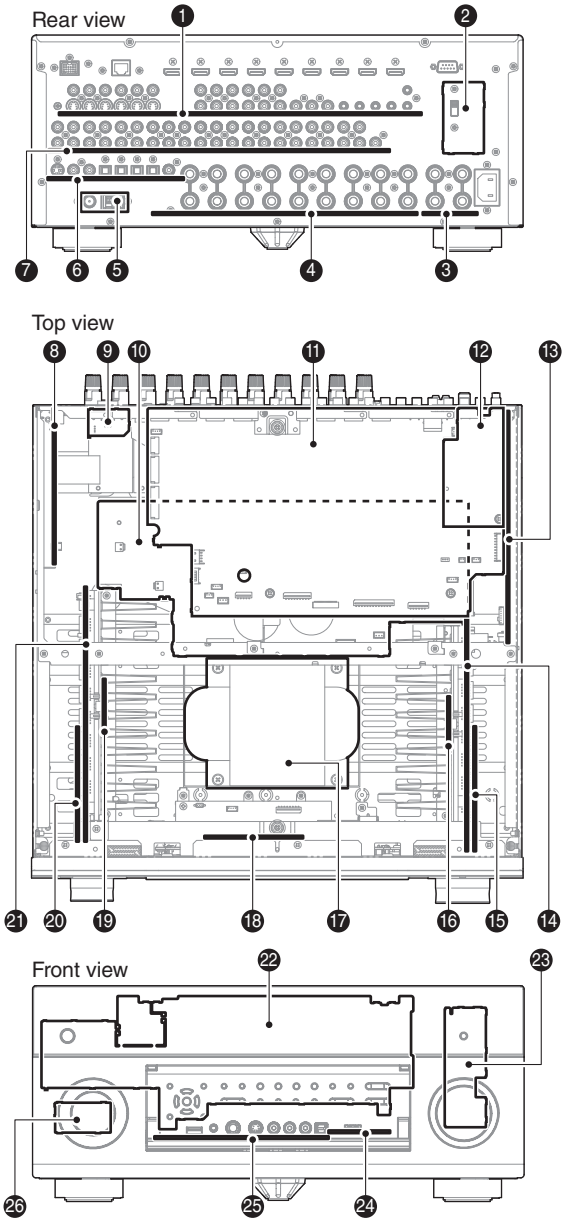
■ INTERNAL VIEW



❶ VIDEO (1) P.C.B.
❷ AMPPOWER (3) P.C.B. (R model)
❸ AMPPOWER (2) P.C.B.
❹ AMP (3) P.C.B.
❺ HD RADIO TUNER (U model)
AM/FM TUNER (C, R, T, K, A, B, G, F, L, J models)
❻ FUNCTION (2) P.C.B.
❼ FUNCTION (1) P.C.B.
❽ POWER P.C.B.
❾ DIGITAL1 (3) P.C.B.
❿ AMPPOWER (1) P.C.B.
⓫ DIGITAL1 (1) P.C.B.
⓬ DIGITAL2 P.C.B.
⓭ DAC P.C.B.
⓮ AMP (2) P.C.B.
⓯ AMPPOWER (5) P.C.B.
⓰ AMP (5) P.C.B.
⓱ POWER TRANSFORMER
⓲ VIDEO (3) P.C.B.
⓳ AMP (4) P.C.B.
⓴ AMPPOWER (4) P.C.B.
㉑ AMP (1) P.C.B.
㉒ OPERATION (1) P.C.B.
㉓ OPERATION (3) P.C.B.
㉔ DIGITAL1 (2) P.C.B.
㉕ OPERATION (2) P.C.B.
㉖ OPERATION (4) P.C.B.

■ SERVICE PRECAUTIONS / サービス時の注意事項

Safety measures

- Some internal parts in this product contain high voltages and are dangerous.
  Be sure to take safety measures during servicing, such as wearing insulating gloves.
- Note that the capacitors indicated below are dangerous even after the power is turned off because an electric charge remains and a high voltage continues to exist there.
  Before starting any repair work, connect a discharging resistor (5 k-ohms/10 W) to the terminals of each capacitor indicated below to discharge electricity.
  The time required for discharging is about 30 seconds per each.

  C1822–C1828 on AMPPOWER P.C.B.

  C2016 on POWER P.C.B.

  For details, refer to “PRINTED CIRCUIT BOARDS”.

安全対策

- この製品の内部には高電圧部分があり危険です。修理の際は、絶縁性の手袋を使用するなどの安全対策を行ってください。
- 下記のコンデンサには電源を OFF にした後も電荷が残り、高電圧が維持されており危険です。
  修理作業前に放電用抵抗（5 k Ω /10 W）を下記の各コンデンサの端子間に接続して放電してください。
  放電所用時間は各々約 30 秒間です。

  AMPPOWER P.C.B. の C1822 ～ C1828

  POWER P.C.B. の C2016

  詳しくは “PRINTED CIRCUIT BOARDS” を参照してください。

Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
86	J10	GND				
87	J11	GND				
88	J12	GND				
89	J13	GND				
90	J14	VDDINT				
91	J19	/AMS0	---			
92	J20	EXT_WAKE0		O	Data	Wake up indication 0
93	K1	PG9/TMR5/RSCLK0A/TACI5	NCPU_PIC_MISO	O	L act	Buffer overflow flag of FPGA
94	K2	PG10/TMR6/TSCLK0A/TACI6	MT_DAC_Z	O	H act	ZONE DAC mute
95	K7	VDDEXT				
96	K8	VDDEXT				
97	K9	GND				
98	K10	GND				
99	K11	GND				
100	K12	GND				
101	K13	GND				
102	K14	VDDINT				
103	K19	/AMS1	---			
104	K20	CLKOUT	BF_CLK	O	Clock	SDRAM clock
105	L1	PG7/TMR3/DR0PRIA/UART0TX	DBG_MOSI	O	Data	UART Tx for Debug
106	L2	PG8/TMR4/RFS0A/UART0RX/ TACI4	DBG_MISO	I	Data	UART Rx for Debug
107	L7	VDDEXT				
108	L8	VDDMEM				
109	L9	GND				
110	L10	GND				
111	L11	GND				
112	L12	GND				
113	L13	GND				
114	L14	VDDINT				
115	L19	VPPOTP				
116	L20	/AMS3	---			
117	M1	PG5/TMR1/PPI_FS2	---	O	L act	
118	M2	PG6/DT0PRIA/TMR2/PPI_FS3	APPLE_I2C_ON	O	H act	APPLE I2C line switch control (H: connect, L: disconnect)
119	M7	VDDMEM				
120	M8	VDDMEM				
121	M9	GND				
122	M10	GND				
123	M11	GND				
124	M12	GND				
125	M13	GND				
126	M14	VDDINT				
127	M19	/AMS2	---			
128	M20	/ARE	BF_N_ARE	O	L act	EBIU read enable
129	N1	PG3/MISO/DR0SECA	BF_SPI_MISO	I	Data	
130	N2	PG4/MOSI/DT0SECA	BF_SPI_MOSI	O	Data	
131	N7	VDDMEM				
132	N8	VDDMEM				
133	N9	GND				
134	N10	GND				
135	N11	GND				
136	N12	GND				
137	N13	GND				
138	N14	VDDINT				
139	N19	/AWE	BF_N_WR	O	L act	EBIU write enable
140	N20	/AOE	---	O	L act	
141	P1	PG1/SPISS/SPISEL1	SFLASH_N_CS	O	L act	SPI flash memory chip select output (L: select)
142	P2	PG2/SCK	BF_SPI_SCK	O	Clock	SPI clock
143	P7	VDDMEM				
144	P8	VDDMEM				
145	P9	VDDMEM				
146	P10	VDDMEM				
147	P11	VDDMEM				
148	P12	VDDINT				
149	P13	VDDINT				
150	P14	VDDINT				
151	P19	ARDY	---	I	H act	
152	P20	SCKE	BF_SCKE	O	H act	SDRAM CKE

Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
153	R1	TDI	BF_JTAG_TDI	I	Data	ICE Debug TDI
154	R2	PG0/HWAIT	BF_JTAG_N_INT	I	Inter-rupt	
155	R19	/SMS	BF_N_SMS	O	L act	SDRAM chip select
156	R20	VDDOTP				
157	T1	TDO	BF_JTAG_TDO	O	Data	ICE Debug TDO
158	T2	/EMU	BF_JTAG_N_EMU	O	Data	ICE Debug /EMU
159	T19	/SRAS	BF_N_SRAS	O	L act	SDRAM /RAS
160	T20	/SWE	BF_N_SWE	O	L act	SDRAM /WE
161	U1	TRST	BF_JTAG_N_TRST	I	L act	ICE Debug /TRST
162	U2	TMS	BF_JTAG_TMS	O	Data	ICE Debug TMS
163	U19	SA10	BF_SA10	O	Data	SDRAM A10
164	U20	/SCAS	BF_N_SCAS	O	L act	SDRAM /CAS
165	V1	DATA15	BF_D[15]	B	Data	Data bus bit 15
166	V2	TCK	BF_JTAG_TCK	I	Clock	
167	V19	/ABE0/SDQM0	BF_SDQM0	O	H act	SDRAM DQM0
168	V20	/ABE1/SDQM1	BF_SDQM1	O	H act	SDRAM DQM1
169	W1	DATA14	BF_D[14]	B	Data	Data bus bit 14
170	W2	DATA13	BF_D[13]	B	Data	Data bus bit 13
171	W3	DATA11	BF_D[11]	B	Data	Data bus bit 11
172	W4	DATA9	BF_D[9]	B	Data	Data bus bit 9
173	W5	DATA7	BF_D[7]	B	Data	Data bus bit 7
174	W6	DATA5	BF_D[5]	B	Data	Data bus bit 5
175	W7	DATA3	BF_D[3]	B	Data	Data bus bit 3
176	W8	DATA1	BF_D[1]	B	Data	Data bus bit 1
177	W9	BMODE3	BMODE3			Boot mode select 3
178	W10	BMODE1	BMODE1			Boot mode select 1
179	W11	ADDR18	BF_A[18]	O	Data	Address bus bit 18
180	W12	ADDR16	BF_A[16]	O	Data	Address bus bit 16
181	W13	ADDR14	BF_A[14]	O	Data	Address bus bit 14
182	W14	ADDR12	BF_A[12]	O	Data	Address bus bit 12
183	W15	ADDR10	BF_A[10]	O	Data	Address bus bit 10
184	W16	ADDR8	BF_A[8]	O	Data	Address bus bit 8
185	W17	ADDR6	BF_A[6]	O	Data	Address bus bit 6
186	W18	ADDR4	BF_A[4]	O	Data	Address bus bit 4
187	W19	ADDR2	BF_A[2]	O	Data	Address bus bit 2
188	W20	ADDR1	BF_A[1]	O	Data	Address bus bit 1
189	Y1	GND				
190	Y2	DATA12	BF_D[12]	B	Data	Data bus bit 12
191	Y3	DATA10	BF_D[10]	B	Data	Data bus bit 10
192	Y4	DATA8	BF_D[8]	B	Data	Data bus bit 8
193	Y5	DATA6	BF_D[6]	B	Data	Data bus bit 6
194	Y6	DATA4	BF_D[4]	B	Data	Data bus bit 4
195	Y7	DATA2	BF_D[2]	B	Data	Data bus bit 2
196	Y8	DATA0	BF_D[0]	B	Data	Data bus bit 0
197	Y9	BMODE2	GND			
198	Y10	BMODE0	+3.3V			
199	Y11	ADDR19	BF_A[19]	O	Data	Address bus bit 19
200	Y12	ADDR17	---			
201	Y13	ADDR15	---			
202	Y14	ADDR13	BF_A[13]	O	Data	Address bus bit 13
203	Y15	ADDR11	---			
204	Y16	ADDR9	BF_A[9]	O	Data	Address bus bit 9
205	Y17	ADDR7	BF_A[7]	O	Data	Address bus bit 7
206	Y18	ADDR5	BF_A[5]	O	Data	Address bus bit 5
207	Y19	ADDR3	BF_A[3]	O	Data	Address bus bit 3
208	Y20	GND				

MEMO